REMARKS

Applicant would like to thank the Examiner for the careful consideration given the present application. The application has been carefully reviewed in light of the Office action, and amended as necessary to more clearly and particularly describe the subject matter which applicant regards as the invention.

Claim 4 has been amended to correct an informality. All other claims remain unchanged.

The Examiner rejected claims 4, 8, and 9 under 35 U.S.C. 103(a) as being unpatentable over Ishizaka, JP-06-111869 in view of Simpson et al., U.S. Pat. No. 5,096,426. The Examiner's rejection is traversed for the following reason.

In regards to claim 4, Applicant discloses a connector chip that includes a rectangular parallelepiped insulating substrate having six surfaces and multiple conductive paths formed on an outer peripheral surface. The conductive paths are continuously formed by four of the six surfaces. Insulating layers having a property of repelling molten solder are formed on opposite surfaces of the substrate between portions of two adjoining conductive paths. The insulating layers are made of an epoxy resin, a glass or the like, which all have the property of repelling molten solder.

Thus, a feature of the present invention is that insulating layers are formed on the outer peripheral surface of the substrate between adjoining conductive paths, which Applicant respectfully contends is not taught by the cited prior art. Further, the insulating layers have the property of repelling molten solder and are made of an epoxy resin, a glass or the like, which Applicant respectfully contends is not taught

by Ishizaka. The insulating layers prevent solder from running between the conductive paths and the electrodes when the electrodes are soldered to the chip thereby preventing an electrical short circuit.

Accordingly, Applicant respectfully contends that Ishizaka, Simpson or the combination thereof do not teach all the features of claim 1. More specifically, Ishizaka, Simpson or the combination thereof do not teach "wherein on at least a pair of the surfaces opposing to each other among the four surfaces, insulating layers having a property of repelling molten solder are formed respectively between portions of two adjoining conductive paths among the plurality conductive paths, located on the pair of the surfaces, and the insulating layers are formed of an epoxy resin, a glass or the like."

In regards to Ishizaka, Ishizaka teaches a terminal 20 that includes an insulator 21 and multiple conductors 22 mounted to the insulator 21 at spaced intervals. The insulator 21 corresponds to the insulating substrate (3) in the present invention and the multiple conductors 22 correspond to the conductive paths (5) in the present invention. The present invention, however, further includes an insulating layer (7) formed on the insulating substrate (3). Ishizaka, on the other hand, does not teach or suggest an insulating layer being formed on the insulator 21. Thus, Ishizaka does not teach an insulating layer, as required by claim 4 of the present invention.

Further, Ishizaka does not teach or suggest that the insulator 21 has molten solder repelling properties. On page 3 of the Office action, the Examiner alluded to the fact that Ishizaka does not teach an insulator having molten solder repelling properties. Thus, the Examiner cited Simpson and stated that Simpson teaches the

use of insulating layers (54) formed of an epoxy resin and that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Ishizaka with Simpson.

In regards to Simpson, Applicant respectfully contends that Simpson does not teach an insulating layer. Rather, Simpson teaches an insulative electrically predetermined sector. Referring to column 4, lines 61-69 and to FIG. 4 of Simpson, Simpson teaches an interconnect element 50 divided into multiple longitudinal sectors. The sectors include two conductive sectors 52, 56 separated by an insulative electrically predetermined sector 54. Thus, the insulative electrically predetermined sector 54 corresponds to the insulating substrate (3) of the present invention and the two conductive sectors 52, 56 correspond to the conductive paths (5) of the present invention. The present invention, however, further includes an insulating layer (7) formed on the insulating substrate (3). Simpson, on the other hand, does not teach or suggest an insulating layer being formed on the insulative electrically predetermined sector 54. Thus, Simpson does not teach an insulating layer, as required by claim 4 of the present invention.

Based on the foregoing, it is apparent that Ishizaka, Simpson or the combination thereof do not teach all the features of claim 4. Thus, reconsideration and withdrawal of the rejections of claim 4 based upon the Ishizaka and Simpson references are hereby requested.

Claims 8 and 9 depend from claim 4, thus, all arguments pertaining to claim 4 are equally applicable to these claims and are herein incorporated by reference.

The Examiner rejected claims 5, and 10 under 35 U.S.C. 103(a) as being unpatentable over Ishizaka, JP-06-111869 and Simpson et al., U.S. Pat. No.

5,096,426, and further in view of Evans, U.S. Pat. No. 3,985,413. The Examiner's rejection is traversed for the following reason.

Claims 5 and 10 depend from claim 4, thus, all arguments pertaining to claim 4 are equally applicable to these claims and are herein incorporated by reference.

Further, Applicant submits that Evans does not correct or eliminate the deficiencies of the primary reference, Ishizaka, as they relate to claim 4. Evans discloses an electrical connector for forming connections between conductors on parallel spaced substrates. Evans, however, does not disclose insulator layers between adjoining conductive paths made from an epoxy resin, glass or the like, as required by claim 4 of the present invention. Thus, Evans does not correct or eliminate the deficiencies of Ishizaka as they relate to claim 4. Therefore, Applicant submits that claims 5 and 10 are allowable over the proposed combination of the references.

The Examiner rejected claim 7 under 35 U.S.C. 103(a) as being unpatentable over Ishizaka, JP-06-111869 and Simpson et al., U.S. Pat. No. 5,096,426, and further in view of Shibata, U.S. Pat. No. 6,123,558. The Examiner's rejection is traversed for the following reason.

Claim 7 depends from claim 4, thus, all arguments pertaining to claim 4 are equally applicable to claim 7 and are herein incorporated by reference.

Further, Applicant submits that Shibata does not correct or eliminate the deficiencies of the primary reference, Ishizaka, as they relate to claim 4. Shibata discloses a card edge connector that includes a slot to receive a circuit card. Shibata, however, does not disclose an insulator layer between adjoining conductive paths made from an epoxy resin, glass or the like, as required by claim 4 of the

present invention. Thus, Shibata does not correct or eliminate the deficiencies of Ishizaka as they relate to claim 4. Therefore, Applicant submits that claim 7 is allowable over the proposed combination of the references.

In light of the foregoing, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in a condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 18-0160, our Order No. NIS-16657.

Respectfully submitted,

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